

REMARKS

In the Office Action, the Examiner rejected claims 1, 4-6, 9-18, 21-24 under 35 USC § 112 and claims 1, 4-6, 9-11, 13-18 and 21-24 under 35 USC § 103. These rejections are fully traversed below.

Claim 5 has been amended. Claim 25 has been added. Claims 19 and 20 have been cancelled. Thus, claims 1, 4-6, 9-18 and 21-25 are pending in the application. Reconsideration of the application is respectfully requested based on the following remarks.

ISSUES UNDER 35 USC 112(1)

Claims 1, 4-6, 9-18, 21-24 have been rejected under 35 USC 112, first paragraph as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The Applicant respectfully disagrees. While the claim limitation “without performing any intervening processing steps between the etching and removal steps” may not appear in the specification in its present form, it should be emphasized that it does indeed have a basis in the original disclosure and thus it does not introduce new concepts. In particular, support for this limitation may be found in the written description of Fig. 2 found on pages 7 and 8, which reads, “The procedure 200 begins at step 202 where a wafer is received by an operator or by a machine. The wafer is generally received for a specific processing task (e.g., step 206). By specific processing task, it is meant that the processing task is the next task (emphasis added) in a sequence of tasks used to process the wafer (lines 2-7)...After receiving the wafer, the process flow proceeds to step 204 where unwanted particles are removed from the backside of the wafer (lines 19-20)...After the unwanted particles have been removed from the backside of the wafer, the process flow proceeds to step 206 where a processing task is performed on the process side of the wafer (lines 13-15).” As should be appreciated, one skilled in the relevant art would most assuredly interpret the term “**next**” as used in the specification to mean immediately following. And if “**next**” means immediately following then no other processing steps can be performed between the processing task and the removal step. The specification goes on to further define a processing task on page 8, lines 22-23, which reads, “the processing task may include etching

deposition or some form of patterning.” One skilled in the art would also interpret the term “include” as used in the specification to mean part of a group where processing task is generic and etching, deposition and patterning are species, i.e., the processing task may be selected from an etching task, a deposition task or a patterning task. It is believed that the Examiner incorrectly applied the courts decisions with regards to the claims to the specification. In the claims, the courts have held that the term “include” is synonymous with “comprising”. This however this is not the case in the specification. In the specification, the meanings of words correspond to how one skilled in the art would interpret them. It should also be noted that the Applicant agrees with the Examiner that the etching, deposition or patterning tasks may include several substeps. This however is irrelevant in that they are all part of the processing task, i.e., the substeps would all occur during the processing task without moving the wafer (while the wafer is on the chucking surface). Accordingly, the rejection should be withdrawn.

With regards to using the transitional phrase “comprising” in the claims, the Applicant respectfully disagrees with the Examiners assertion that “comprising” makes the limitation “without performing any intervening processing steps between the etching and removal steps” meaningless since the word “comprising” permits the introduction of any process steps. “Comprising” is the term of art used in claim language which means the named elements are essential, but other elements may be added and still form a construct within the scope of the claim. See *Genetech, Inc. v Chiron Corp.*, 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997). In the claims, the essential element is that no intervening processing steps are performed between the etching and removal steps. This element does not limit the addition of other elements. For example, other processing steps may be performed before the removal steps. Furthermore, other non processing steps may be performed between the etching and removal steps (e.g., placing the wafer on a chucking surface).

ISSUES UNDER 35 USC 102(b)

Claims 5, 6, 9, 10, 14 and 15 have been rejected under 35 U.S.C. §102(b) as being anticipated by *La et al.* (U.S. Patent No. 6,136,510).

In contrast to *La*, claim 5 (and its dependents) specifically requires, “...performing a processing sequence consisting of loading the wafer into the cleaning module; cleaning the backside of the wafer in the semi-dry cleaning module to remove particles therefrom, wherein

only the backside of the wafer is cleaned in the semi dry cleaning module so as not to damage the process side of the wafer; transferring the wafer to the processing module; loading the wafer into the processing module; and etching the process side of the wafer in the processing module while the wafer is inside the processing module.”. While *La* may disclose scrubbing and an etching step, *La* also discloses performing a photolithographic technique between the scrubbing and etching steps. Scrubbing does **not** occur between the photolithographic technique and the etching step (See Col. 5, lines 16-45). This goes against the limitation of claim 5 described above. In fact, because of this one may argue that *La* teaches away from the above mentioned limitations. As stated in the specification of the present invention, on page 2, lines 27-30, “...with regards to trapped particles, the particles may be dust, polymer deposits and/or **excess photoresist** that has accumulated or collected on the backside of the wafer and/or top surface of the chuck during prior processing steps and/or transfers.” In the sequence of *La*, excess photoresist may adhere to the backside of the wafer between the scrubbing and etching steps since the photolithographic technique occurs therebetween. This excess photoresist may lead to problems, which the present invention is trying to prevent by excluding intervening steps between the cleaning and etching steps (e.g., maintaining the desired relationship between the backside of the wafer and the top surface of the chuck). Accordingly, the rejection is unsupported by the art and should be withdrawn.

Also in contrast to *La*, claim 5 (and its dependents) specifically requires, “...wherein only the backside of the wafer is cleaned in the semi dry cleaning module so as not to damage the process side of the wafer...” While *La* may disclose scrubbing the backside of the wafer, *La* does not teach or suggest scrubbing only the backside of the wafer. In *La*, both sides of the wafer are scrubbed. *La* repeatedly states that his invention comprises a less severe and more cost effective solution for reducing photolithographic failures by performing a double-sided scrubbing operation using conventional in place equipment. For example, *La* states, “The present invention addresses and solves the problem in a cost effective and efficient manner, preferably by utilizing existing production equipment. The solution ...resides in scrubbing the backside of the wafer preferably by performing a double sided scrubbing operation at strategic times...(Col. 3. lines 41-48).” See also Col. 3, lines 59-62, where *La* teaches away from CMP of the wafer backside by expressly stating that a double sided scrubbing operation is performed.

The Examiner asserted that *La* teaches an embodiment of “only backside scrubbing” in Col. 4 lines 1-6. The Applicant respectfully disagrees. This section is not an embodiment

teaching only backside scrubbing. It is not a preferred embodiment. It is not a less preferred embodiment. It is not even a non preferred embodiment. *La* only teaches a double sided scrubbing operation. With regards to the phrase “backside scrubbing is effected by processing only the backside of the wafer by a scrubbing operation”, close attention must be made to see how the sentence is constructed. *La* is not stating that backside scrubbing is performed without front side scrubbing. *La* is simply defining the term “backside scrubbing” to mean that only the backside of the wafer is processed during backside scrubbing. The term “only” is being used to define backside scrubbing, it is not being used to exclude front side scrubbing. If *La* was in fact describing a different embodiment (e.g., other than double sided scrubbing), then “backside scrubbing” should have been replaced with “scrubbing.” This phrase simply does not exclude front side scrubbing from the overall scrubbing operation as is required by claims 5. Furthermore, taken in context with the aim of the invention it is believed that one skilled in the art would not interpret this sentence to preclude front side scrubbing. This goes against what is being taught throughout *La* (e.g., double sided scrubbing). Accordingly, the rejection is unsupported by the art and should be withdrawn.

Although the rejections to the dependent claims 6, 9, 10, 14 and 15 should be withdrawn for at least the reasons as above, it should be noted that they offer additional language that is unsupported by the art.

ISSUES UNDER 35 USC 103(a)

Claims 1, 4, 11, 12, 16-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *La* et al. (U.S. Patent No. 6,136,510) in view of *Guo* et al. (U.S. Patent No. 6,251,759).

Guo does not overcome the deficiencies of *La*. That is, while *La* may disclose scrubbing and etching steps and *Guo* may disclose process chambers and preclean chambers, neither reference teaches or suggests “etching the process side of the wafer...without performing any intervening processing steps between etching and removal steps,” as required by claim 1 (and its dependents), and “...performing a processing sequence consisting of ...” as required by claim 5 from which claim 11, 12 and 16-18 depend. See arguments above with regards to *La*. With regards to *Guo*, *Gou* is completely silent to etching and removal steps. The most that can be said is that *Gou* discloses depositing copper using metallization or sputtering techniques and

including preclean chambers. *Guo* does not describe the preclean chambers in any detail. Accordingly, the rejection is unsupported by the art and should be withdrawn.

Also in contrast to *La* and *Guo*, claim 5 (from which claims 11, 12 and 16-18 depend) specifically requires, "...wherein only the backside of the wafer is cleaned in the cleaning module so as not to damage the process side of the wafer..." With regards to *Guo*, *Guo* is silent to cleaning the backside of the wafer. In *La*, both sides of the wafer are scrubbed (see arguments above). Accordingly, the rejection is unsupported by the art and should be withdrawn.

Claims 1, 4, 11, 13 and 16-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *La* et al. (U.S. Patent No. 6,136,510) in view of *Loan* et al. (U.S. Patent No. 6,136,725).

Loan does not overcome the deficiencies of *La*. That is, neither reference teaches or suggests, "etching the process side of the wafer...without performing any intervening processing steps between etching and removal steps," as required by claim 1, "...performing a processing sequence consisting of ..." as required by claim 5 from which claims 11, 13 and 16-18 depend, and further, "...wherein only the backside of the wafer is cleaned in the cleaning module so as not to damage the process side of the wafer..." as required by claim 5 from which claims 11, 13 and 16-18 depend. With regards to *La*, see arguments made above. With regards to *Loan*, *Loan* is directed at deposition rather than etching and further does not teach or suggest sequential cleaning steps associated with a wafer. Accordingly, the rejection is unsupported by the art and should be withdrawn.

Claim 21-24 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *La* in view of *Hiatt* (U.S. 5,966,635) and in further view of *Fukasawa* (U.S. 5 310,453).

The rejection should be withdrawn for at least the reasons given above (e.g., claim 21 has similar limitation to claims 1 and 5). That is, none of the references teach or suggest "providing a cleaning module for cleaning the backside of the wafer and a plasma reactor for performing an etching task...removing the wafer from the cleaning module and thereafter introducing the wafer into the process chamber of the plasma reactor without performing any intervening processing steps therebetween..." or "...wherein only the backside is cleaned so as not to damage the process side of the wafer..." as required by claim 21. See argument above with regards to *La*.

Hiatt and *Fukasawa* do not overcome the deficiencies of *La. Hiatt* and *Fukasawa* fail to disclose removing residual material from a wafer. The most that can be said is that *Hiatt* discloses applying a solvent to the surface of a chuck to remove residual material that adheres to the surface of the chuck. Accordingly, the rejection is unsupported by the art and should be withdrawn.

Although the rejections to the dependent claims 22-24 should be withdrawn for at least the reasons as above, it should be noted that they offer additional language that is unsupported by the art.

SUMMARY

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

A handwritten signature in black ink, appearing to read "Hoellwarth", with a stylized initial "Q" or "H" at the start.

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